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SEMICONDUCTOR MEMORY DEVICE HAVING OFFSET TRANSISTOR AND METHOD OF FABRICATING THE SAME

Field of the Invention

The present invention generally relates to a semiconductor memory device and a method for fabricating the same. More specifically, the present invention is directed to a semiconductor memory device having an offset transistor and method of fabricating the same.

Background of the Invention

DRAM device has a higher density of integration than SRAM device, but should be performed a refresh operation for preventing data loss. As a result, a DRAM device consumes a power during even a stand-by mode. On the contrary, it is not necessary to perform the refresh process in a nonvolatile memory device such as a flash memory device. However, the nonvolatile memory device needs a high voltage to perform a write operation.

In order to overcome the drawbacks of DRAMs and nonvolatile memory devices, semiconductor memory devices using multi-tunnel junction patterns are suggested, for example, in U.S. Pat. No.5,952,692, entitled "Memory Device With Improved Charge Storage Barrier Structure" and U.S. Pat. No.6,169,308, entitled "Semiconductor Memory Device And Manufacturing Method Thereof". An example of such semiconductor memory devices using multi-tunnel junction patterns is shown Figs 1 and 2, which are a cross-sectional view and a circuit diagram thereof, respectively.

Referring to Figs. 1 and 2, a unit cell of a semiconductor memory

device comprises a vertical transistor TR1 and a planar transistor TR2. The planar transistor TR2 comprises a source region 39s, a drain region 39d and floating gate 6, where the source/drain regions 39s and 39d are formed in a predetermined region of a semiconductor substrate 2 to be spaced apart from each other and the floating gate 6 is disposed on the channel region between the source and drain regions 39s and 39d. Here, the drain region 39d corresponds to a bit line and the floating gate 6 corresponds to a storage node. A gate insulator 4 is interposed between the storage node 6 and the channel region.

A multi-tunnel junction pattern 16 and a data line 27 are sequentially stacked on the storage node 6. The multi-tunnel junction pattern 16 comprises a semiconductor layer 8 and a tunnel insulating layer 10 stacked repeatedly and sequentially. Here, an utmost top layer 12 of the multi-tunnel junction pattern 16 may be the semiconductor layer 8 or the tunnel insulating layer 10. The data line 27 extends to connect electrically with a plurality of an adjacent memory cells. The storage node 6, the multi-tunnel junction pattern 16 and the data line 27 constitute a multi-layered pattern.

A gate inter-layered insulator 40 covers the side and top surfaces of the multi-layered pattern. A word line 42 is disposed on the gate inter-layered insulator 40 to cross the data line 27 and other multi-layered patterns. The data line 27, the multi-tunnel junction pattern 16, the storage node 6 and the word line 42 constitute the vertical transistor TR1.

The operating method of the semiconductor memory cell described above will be explained from now.

First, a data voltage and a write voltage are applied to the data line 27

and the word line 42 during a writing mode, respectively. Thus, an inversion channel is formed at the sidewalls of the semiconductor layer 8 to generate a tunneling current flowing through the tunnel insulating layer 10. As a result, electric charges such as electrons and holes are stored in the storage node 6 to change the threshold voltage of the planar transistor TR2, where the quantity of electric charges depends on a voltage applied to the data line 20.

Next, for reading data stored in the storage node 6, a reading voltage is applied to the storage node 6 and a suitable voltage, for example the ground voltage, is applied to the source region 39s. If a threshold voltage of the planar transistor TR2 is higher than the reading voltage, the planar transistor TR2 becomes a turn-off state. Thus, no current flows through the drain region 39d. On the contrary, if the threshold voltage of the planar transistor TR2 is lower than the reading voltage, the planar transistor TR2 becomes a turn-on state to flow some current through the drain region 39d. The storage node 6 plays a role of the gate of the planar transistor TR2 during the reading operation, and the reading voltage applied to the storage node 6 depends on a voltage applied to the word line 42 and a coupling ratio.

According to the above-described prior art, during the writing operation, the threshold voltage of the planar transistor TR2 are changed depending on a quantity of electric charges stored in the storage node 6. Meanwhile, the reading operation comprises sensing a quantity of electric charges flowing through the channel region of the planar transistor TR2, where the quantity of electric charges changes dependent on the threshold voltage of the planar transistor TR2. However, if electric charges stored in the storage node 6 are insufficient, a higher voltage is needed for the word

line in the reading operation. If the voltage applied to the word line is higher, a channel region is formed in the vertical transistor to cause a leakage of the electric charges stored in the storage node 6.

Summary of the Invention

It is therefore a feature of the present invention to provide a semiconductor memory device having a characteristic of an excellent reading operation in a low operation voltage.

It is another feature of the present invention to provide a method of fabricating a semiconductor memory device having a characteristic of an excellent reading operation in a low operation voltage.

It is another feature of the present invention to provide a semiconductor memory device preventing a leakage of electric charges in a storage node.

It is still another feature of the present invention to provide a method of fabricating a semiconductor memory device preventing a leakage of electric charges in a storage node.

A unit cell of a semiconductor memory device according to an embodiment of the present invention comprises two planar transistors and one vertical transistor. A first planar transistor comprises a first conductive region, a second conductive region, a first channel region, a second channel region and a storage node. Here, the first and second conductive regions are disposed in a predetermined region of a semiconductor substrate to be parallel with each other, the first and second channel regions are disposed between the first and second conductive regions and the storage node is

disposed on the first channel region. A gate insulating pattern is interposed between the storage node and the first channel region. A vertical transistor comprises the storage node, a multi-tunnel junction pattern stacked on the storage node, a data line stacked on the multi-tunnel junction pattern, and a word line crossing the data line and covering sidewalls of the storage node and the multi-tunnel junction pattern. The word line crosses the second channel region to form a second planar transistor. The storage node plays roles of a gate electrode of the first planar transistor and a source region of vertical transistor. During a reading operation of this structure, a voltage of the word line is applied depending on the coupling ratio to the first planar transistor as a read voltage, while the voltage of the word line is directly applied to the second planar transistor. Therefore, a leakage of electric charges in a storage node can be minimized, because the reading operation can be performed in a low voltage of the word line.

A method of fabricating the semiconductor memory device according to an embodiment of the present invention comprises forming a gate insulator pattern, a storage node, a multi-tunnel junction pattern and a data line sequentially stacked on a first channel region of a semiconductor substrate. The data line is extended along a specific direction. Next, a mask pattern is formed to define the second channel region and a first conductive region and a second conductive region is formed in the semiconductor substrate using the mask pattern as an ion implantation mask, wherein the first and second conductive regions are spaced as long as the width of a second channel region. The mask pattern is removed and a gate interlayer insulating layer is conformally formed on the entire surface of the

semiconductor substrate having the storage node. A plurality of word lines are formed to cross the data lines on the gate interlayer insulating layer and to be parallel to each other. Here, the word line crosses the storage node and the multi-tunnel junction pattern to form the vertical transistor and crosses the second channel region to form a gate electrode of the second planar transistor.

Brief Description of the Drawings

Fig. 1 is a cross-sectional view illustrating a semiconductor memory device having a multi-tunnel junction pattern according to prior art.

Fig. 2 is a circuit diagram illustrating a unit cell of a semiconductor memory device having a multi-tunnel junction pattern according to prior art.

Fig. 3 is a top plan view illustrating a part of a cell array region of a semiconductor memory device according to the present invention.

Fig. 4a is a cross-sectional view illustrating a semiconductor memory device taken along the line I-I of Fig. 3.

Fig. 4b is a cross-sectional view illustrating a semiconductor memory device taken along the line II-II of Fig. 3.

Fig. 5 is a circuit diagram illustrating a unit cell according to the present invention.

Figs. 6a-12a and Figs. 6b-12b are cross-sectional views illustrating a method for fabricating a semiconductor memory device according to an embodiment of the present invention.

Description of the Preferred Embodiment

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. It will also be understood that when a layer is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Like numbers refer to like elements throughout.

Fig. 3 is a top plan view illustrating a part of a cell array region of a semiconductor memory device according to the present invention. Figs. 4a and 4b are cross-sectional views of a semiconductor memory device taken along the line I-I and the line II-II of Fig. 3. Fig. 5 is a circuit diagram of a unit cell according to the present invention

Referring to Figs. 3, 4a, 4b and 5, a first conductive region 139d and a second conductive region 139s are disposed in a predetermined region of a semiconductor substrate 102 to be parallel to each other. The first and second conductive regions 139d and 139s are parallel with a specific direction, for example, a row direction. And a first channel region L1 and a second channel region L2 are interposed between the first and second conductive regions 139d and 139s. The first conductive region 139d is connected with a sense amplifier (not shown) to be used as a bit line.

Pluralities of multi-layered patterns are disposed along the column direction on the semiconductor substrate 102 between the first and second conductive regions 139d and 139s. The region between the multi-layered patterns is filled with an isolation pattern 124. Here, the isolation pattern 124 is extended into the semiconductor substrate 102 to isolate the adjacent multi-layered patterns. Each of the multi-layered patterns comprises a storage node 106 and a multi-tunnel junction pattern 116 stacked sequentially.

The multi-tunnel junction pattern 116 comprises a semiconductor layer pattern 108 and a tunnel insulating pattern 110 stacked repeatedly and sequentially. An utmost top layer of the multi-tunnel junction pattern 116 may be a storage node 106 or a multi-tunnel junction pattern 116.

A data line is disposed on the multi-tunnel junction pattern 116 and the isolation pattern 124 interposed between the multi-tunnel junction patterns 116. Thus, the data line 127 is disposed between the first and second conductive regions 139d and 139s. A capping insulation pattern 128 may be disposed in the data line 127. A plurality of parallel word lines 142 cross over the data line 127. Each of the word lines 142 covers both sidewalls of the storage node 106, both sidewalls of the multi-tunnel junction pattern 116 and the top surface of the second channel region L2. A conformal gate interlayer insulating layer 140 is interposed between the word lines 142 and the storage node 106, between the word lines 142 and the multi-tunnel junction pattern 116 and between the word lines 142 and the second channel region L2.

The semiconductor memory device having the above mentioned structure comprises one vertical transistor TR1 and two planar transistors

TR2a and TR2b. The first planar transistor TR2a comprises the first and second conductive regions 139a and 139b, the first and second channel regions L1 and L2 and the storage node 106. The first and second channel regions L1 and L2 are interposed between the first and second conductive regions 139d and 139s and the storage node 106 is disposed on the first channel region L1, as stated above. The vertical transistor TR1 comprises the storage node 106, the multi-tunnel junction pattern 116, the data line 127 and the word line 142. Here, as abovementioned, the multi-tunnel junction pattern 116 is disposed on the storage node 106 and the data line 127 is disposed on the multi-tunnel junction pattern 116 to be parallel with the first and second conductive regions 139d and 139s. And, the word line 142 is disposed across the data line 127 to cover both sidewalls of the storage node 106 and the multi-tunnel junction pattern 116. Preferably, the word line 142 is disposed across the second channel region L2 to be used as the gate electrode of the second planar transistor TR2b. The second planar transistor TR2b is disposed adjacent to the first planar transistor TR2a and on the second channel region L2 to be an offset transistor. A reference number 132 in Fig. 3 denotes a mask pattern for defining the second channel region L2 of the second planar transistor TR2b.

Figs. 6a-12a and Figs. 6b-12b are cross-sectional views illustrating a fabricating method of a semiconductor memory device according to an embodiment of the present invention. Figs. 6a-12a are cross-sectional views taken along the line I-I of Fig. 3 and Figs. 6b-12b are cross-sectional views taken along the line II-II of Fig. 3.

Referring to Fig. 6a and 6b, a gate insulating layer 104, a storage

node layer 106, a multi-tunnel junction layer 116, an upper conductive layer 118 and a polishing preventive layer 120 are sequentially formed on a semiconductor substrate 102.

The multi-tunnel junction layer 106 is formed by stacking repeatedly and sequentially a semiconductor layer 108 and a tunnel insulating layer 110. The semiconductor layer 108 may be formed of a silicon layer and the tunnel insulating layer 110 may be formed of a silicon nitride layer, a silicon oxynitride layer or a silicon oxide layer. The utmost top layer 112 of the multi-tunnel junction layer 106 may be the semiconductor layer 108 or the tunnel insulating layer 110. Preferably, the upper conductive layer 118 is formed of a doped silicon layer and the polishing preventive layer 120 is formed of a silicon nitride layer.

Referring to Fig. 7a and 7b, the polishing preventive layer 120, the upper conductive layer 118, the multi-tunnel junction layer 116, the storage node layer 106 and the gate insulating layer 104 are sequentially patterned to form openings exposing a predetermined region of the semiconductor substrate 102. The openings are 2-dimensionally arranged with a column direction and a row direction. Next, the exposed semiconductor substrate is etched to form a plurality of trench regions 122. Therefore, the trench regions are 2-dimensionally arranged to define mesh-shaped active regions likewise.

Referring to Fig. 8a and 8b, an isolating layer is formed on the semiconductor substrate having the trench regions 122 to fill the trench regions 122. Next, the isolating layer is etched until the polishing preventive layer 120 is exposed, to form a plurality of island-shaped isolating patterns

124 filling the trench regions 124. That is, the isolating patterns 124 are also 2-dimensionally arranged along the column and row directions. Preferably, a chemical-mechanical polishing process is performed for the above etching process of the isolating layer. Subsequently, the exposed polishing preventive layer 120 is removed to expose the upper conductive layer 118.

An interconnecting layer and a capping insulation layer are sequentially formed on the resultant structure having the exposed upper conductive layer 118. The interconnecting layer is formed of a metal layer, a polycide layer or a doped silicon layer, and the capping insulation layer is formed of a silicon oxide layer or a silicon nitride layer, preferably. The capping insulation layer, the interconnecting layer and the upper conductive layer 118 are sequentially patterned to form a plurality of a capping insulation pattern 128 and a plurality of a data line 127. Here, the capping insulation patterns 128 are parallel to the row direction and the data lines 127 are disposed beneath the capping insulation patterns 128.

The data lines 127 cover a predetermined region of the isolating patterns 124 which is placed on row directional lines. And, the data line 127 comprises an interconnection line 126 disposed beneath the capping insulation pattern 128 and an upper conductive pattern 118 interposed between the interconnection line 126 and the multi-tunnel junction layer 116. The processing step for forming the upper conductive layer 118 may be omitted when the interconnecting layer is formed of the doped silicon layer or the polycide layer.

Referring to Figs. 9a and 9b, the exposed multi-tunnel junction layer 116 between the data lines 127 is etched to form a plurality of multi-tunnel

junction patterns 116. The multi-tunnel junction patterns 116 are disposed among the isolating patterns 124 and beneath the data lines 127. Here, the multi-tunnel junction pattern 116 comprises a semiconductor pattern 108 and a tunnel insulating pattern 110 stacked repeatedly and sequentially. Continuously, the storage node layer 106 and the gate insulating layer 104 among the data lines 127 are sequentially etched to form a storage node pattern 106 under the multi-tunnel junction patterns 106 and a gate insulating pattern 104 under the storage node patterns 106.

An ion implantation process using the stack-type multi-patterns as a mask may be performed in order to adjust a threshold voltage of the second planar transistor TR2b.

A first mask pattern 132 defining a second channel region is formed after the ion implantation process for adjusting a threshold voltage of the second planar transistor TR2b. Another ion implantation process using the first mask pattern 132 as a mask is performed to form a lightly doped drain region 134 in the semiconductor substrate. The first mask pattern 132 covers the second channel region, in order to prevent from changing a threshold voltage of the second planar transistor TR2b.

Referring to Fig. 10a and 10b, a spacer insulating layer is conformally formed on the substrate removed the first mask pattern 132. The spacer insulating layer is anisotropically etched to form a spacer 135 on the sidewalls of the multi-patterns. Subsequently, a second mask pattern 136 for defining a second channel region is formed on a predetermined region of the semiconductor substrate. A heavily doped region 138 is formed in the semiconductor substrate using the spacer 135, the multi-patterns and the

second mask pattern 136 as an ion implantation mask. Here, the lightly doped drain region 134 and the heavily doped region 138 constitute a first conductive region 139d and a second conductive region 139s. In particular, due to the spacer 135, the heavily doped region 138 and lightly doped drain region 134 of the first conductive region 139d are arranged in a row.

Referring to Figs. 11a and 11b, a gate interlayer insulating layer 140 is conformally formed on the resultant structure having the first and second conductive regions 139d, 139s. The gate interlayer insulating layer 140 may be formed of at least one of combinations consisting of silicon oxide and silicon nitride layer. An etch stop layer (not shown), such as a silicon nitride layer, may be additionally formed on the gate interlayer insulating layer 140. Continuously, an interlayer dielectric 141 is formed on the semiconductor substrate having the gate interlayer insulating layer 140 and the etch stop layer.

Referring to Figs. 12a and 12b, the interlayer dielectric 141 is patterned until exposing the etch stop layer. Thus, a plurality of grooves are formed in the interlayer dielectric 141 to cross over the data lines 127. And the exposed etch stop layer is etched to expose the gate interlayer insulating layer 140. A plurality of word lines 142 are formed in the grooves by performing a conventional damascene process. Each of the word lines 142 covers both sidewalls of the storage nodes 106, both sidewalls of the multi-tunnel junction patterns 116 and the top surface of the second channel region L2. And the word lines 142 are disposed across the second channel region L2 to be used as the gate electrode of the second planar transistor. The reference index L1 in Fig. 12a denotes the first channel region.

According to the present invention, due to the offset transistor, an operation voltage of a semiconductor memory device can be decreased during a reading procedure. And, the reading procedure of the semiconductor memory device can be effectively performed by controlling the threshold voltages of two planar transistors.

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a first planar transistor including a first and second conductive regions, a first and second channel regions and a storage node, wherein the first and second conductive regions are disposed in a predetermined region of a semiconductor substrate to be parallel with each other, the first and second channel regions are disposed between the first and second conductive regions and the storage node is disposed on the first channel region; and

a vertical transistor including the storage node, a multi-tunnel junction pattern stacked on the storage node, a data line stacked on the multi-tunnel junction pattern, and a word line crossing the data line and covering sidewalls of the storage node and the multi-tunnel junction pattern,

wherein the word line crosses the second channel region to form a second planar transistor.

2. The semiconductor memory device of claim 1, further comprising a gate insulating pattern interposed between the storage node and the first channel region.

3. The semiconductor memory device of claim 1, wherein the first planar transistor and the second planar transistor have different threshold voltages with each other.

4. The semiconductor memory device of claim 1, further

comprising a gate interlayer insulator interposed between the word line and sidewalls of the storage node, between the word line and sidewalls of the multi-tunnel junction pattern and between the word line and the second channel region.

5. The semiconductor memory device of claim 1, further comprising a capping insulation pattern interposed between the data line and the word line.

6. The semiconductor memory device of claim 1, wherein the first conductive region comprises a lightly doped drain region and a heavily doped region.

7. The semiconductor memory device comprising:

a first conductive region and a second conductive region disposed parallel with each other in a semiconductor substrate;

a first channel region and a second channel region disposed between the first conductive region and the second conductive region;

a plurality of storage nodes disposed on the first channel region;

a plurality of trench regions disposed in the semiconductor substrate between the storage nodes which is parallel with the first and second conductive regions;

a plurality of multi-tunnel junction pattern stacked on the storage nodes;

isolation layers filling the trench regions;

a plurality of data lines disposed between the conductive regions to cover the multi-tunnel junction patterns and the isolation layers between them; and

a plurality of word lines, which are parallel to each other across the data lines, wherein the word lines cover the sidewalls of the storage nodes, the sidewalls of the multi-tunnel junction patterns and the second channel region.

8. The semiconductor memory device of claim 7, further comprising gate insulating patterns interposed between the storage nodes and the semiconductor substrate.

9. The semiconductor memory device of claim 7, further comprising a capping insulation pattern interposed between the data line and the word line.

10. The semiconductor memory device of claim 7, further comprising a gate interlayer insulating layer interposed between the word line and the sidewall of the storage node, the word line and the sidewall of the multi-tunnel junction pattern, and the word line and the second channel region.

11. The semiconductor memory device of claim 7, wherein the first channel region and the second channel region are different from each other in doping concentrations.

12. The semiconductor memory device of claim 7, wherein the first conductive region comprises a lightly doped drain region and a heavily doped region.

13. A method of fabricating the semiconductor memory device comprising:

forming multi-layered patterns including a gate insulator pattern, a storage node and a multi-tunnel junction pattern sequentially stacked on a first channel region of a semiconductor substrate;

forming a data line on the multi-layered patterns;

forming a first conductive region and a second conductive region at both sides of the storage node respectively, wherein the first conductive region and the second conductive region are spaced as long as the width of a second channel region;

conformally forming a gate interlayer insulating layer on the entire surface of the semiconductor substrate having the storage node; and

forming a plurality of word lines, which are parallel to each other across the data lines, on the gate interlayer insulating layer,

wherein each of the word lines crosses the storage node, the multi-tunnel junction pattern and the second channel region.

14. The method of claim 13, wherein forming the first conductive region and the second conductive region comprises:

forming a mask pattern defining the second channel region;

forming a first conductive region and a second conductive region in the semiconductor substrate using the mask pattern and the multi-layered patterns as an ion implantation mask, wherein the first and second conductive regions are spaced as long as the width of a second channel region; and

removing the mask pattern.

15. The method of claim 14, further comprising an ion implantation process for adjusting a threshold voltage prior to forming the mask pattern.

16. The method of claim 13, wherein forming the first conductive region and the second conductive region comprises:

forming a first mask pattern defining the second channel region;

forming a lightly doped drain region in the semiconductor substrate by performing an ion implantation using the first mask pattern and the multi-layered patterns as an ion implantation mask;

removing the first mask pattern;

forming a spacer on the sidewalls of the multi-layered patterns;

forming a second mask pattern defining the second channel region;

forming a heavily doped region in the semiconductor substrate by performing another ion implantation using the second mask pattern, the multi-layered patterns and the spacer as an ion implantation mask; and

removing the second mask pattern.

17. The method of claim 16, further comprising an ion implantation process for adjusting a threshold voltage prior to forming the first mask pattern.

18. The method of claim 13, further comprising forming an upper conductive pattern between the multi-layered patterns and the data line.

Abstract of the Disclosure

A semiconductor memory device having an offset transistor and method of fabricating the same are provided. The semiconductor memory device comprises a unit cell having two planar transistors and one vertical transistor. A first planar transistor is composed of a first and second conductive regions disposed in a predetermined region of a semiconductor substrate, a first and second channel regions disposed between the first and second conductive regions, and a storage node disposed on the first channel region. The vertical transistor is composed of the storage node, a multi-tunnel junction pattern stacked on the storage node, a data line stacked on the multi-tunnel junction pattern, and a word line covering sidewalls of the storage node and the multi-tunnel junction pattern. The word line crosses over the second channel region to be a gate of a second planar transistor.